Remarks

Claims 1-4 are pending in the application without amendment. No new matter has been added.

In the following text, specific references to the present application and the prior art are made using the notation "x:y", where "x" denotes the page or column number, and "y" indicates the line number, within the document being discussed.

Status of Claims

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McTeer (US 5,700,718).

Response to Rejections Under 35 U.S.C. § 103(a)

Currently, claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McTeer (US 5,700,718).

Claim 1 recites:

> A method of constructing a metallization structure on a preexisting dielectric layer of an integrated circuit during fabrication of the integrated circuit, the method comprising the steps of:
>
> depositing a layer of titanium onto the preexisting dielectric layer of the integrated circuit;
>
> depositing a layer of aluminum onto the layer of titanium;
>
> heating the integrated circuit sufficiently to cause the layer of titanium to become at least partially alloyed with the layer of aluminum; and
>
> further heating the integrated circuit at 400 degrees C for about 45 minutes so that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit.

Concerning claim 1, the examiner has indicated that McTeer discloses all of the recited steps of the method except for the step "further heating the integrated circuit at 400 degrees C for about 45 minutes". The examiner indicates, however, that McTeer discloses "further heating the integrated circuit but fails to teach doing the heating at 400 degrees C for about 45 minutes" (Office Action B, 2:20 - 2:21). The examiner states that "since McTeer teaches the further heating for curing the defects, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the heating temperature and the

duration through routine experimentation and optimization to obtain optimal curing of defects because the heating temperature and duration are result-effective variables and there is no evidence indicating that they are critical or produce any unexpected results...." (Office Action B, 2:22 - 3:1).

The Applicant stands by the arguments set forth in Amendment A, and respectfully wishes to provide further explanation to the Examiner in response to the Examiner's Response to Arguments set forth in Office Action B, 3:17 - 4:5.

McTeer does not teach or suggest the limitation "so that impurities from the dielectric layer *have passivated structural defects* within a silicon layer of the integrated circuit" as recited in Applicant's Claim 1. As stated in the remarks of Amendment A, McTeer teaches only that voids formed in the metal stack are reduced as a result of McTeer's technique (McTeer, 3:45 - 3:51). The reduction of voids in the metallization stack as described in McTeer is not the same as passivating structural defects in the silicon layer of the integrated circuit, as recited in Applicant's Claim 1. In the case of reduction of voids, the size of the voids are made smaller, *but the existing reduced voids still have dangling bonds that facilitate electron flow and therefore allow unwanted leakage current*. In the case of passivation, Applicant's invention exploits the mobile impurities to bind with the dangling bonds of the structural defects, thereby *reducing leakage current*. Therefore, although McTeer states that the wafer undergoes a final anneal process such as that of the prior art which is conducted in a furnace at conventional temperatures and for a conventional amount of time, there is nothing in McTeer that teaches or suggests that passivation of structural defects within a silicon layer of the integrated circuit either occur or would occur as a result of the anneal step.

In Office Action B (3:20 - 3:27), the Examiner asserts that the Applicant's limitation "so that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit" would inherently occur if the further heating of McTeer is done at 400° C for about 45 minutes. However, as agreed to by the Examiner, McTeer *does not teach* "further heating the integrated circuit at 400 degrees C for about 45 minutes". Also in Office Action B (2:22 2:26), the Examiner asserts that it would have been obvious to one of ordinary skill in the art of making

semiconductor devices to determine the workable or optimal value of the heating temperature and duration through routine experimentation and optimization to obtain optimal curing of defects.

In addition, as held in *In re Spormann*, 363 F.2d 444 at 448, 150 USPQ 449 at 452 (C.C.P.A. 1966), "the inherency of an advantage and its obviousness are entirely different questions. That which may be inherent is not necessarily known. Obviousness cannot be predicated on what is unknown". Spormann holds that arguments based on inherent properties cannot stand when there is no supporting teaching in the prior art of the principles or properties said to be inherent. First, McTeer does not teach the principle or property of "passivated structural defects within a silicon layer of the integrated circuit" that is said to be inherent by the Examiner. Second, if experimentation is required, as submitted by the Examiner, then it cannot be said the McTeer provides any supporting teaching that even the correct temperature and duration would be obtained to allow such passivation of structural defects.

It has further been held that "'[i]nherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient.'" *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981) (*quoting Hansgirg V. Kemmer*, 102 F.2d 212, 214, 40 USPQ 665, 557 (C.C.P.A. 1939) (emphasis in original). McTeer simply does not teach either the passivation of structural defects or the temperature and duration claimed in Applicant's claim 1. Therefore, there is nothing in McTeer that supports the limitation "that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit" would inherently occur. Therefore, the Examiner has not met the prima facie case that McTeer teaches this element, and accordingly an obviousness-type rejection cannot stand based on inherency of the property of passivation of structural defects based on McTeer.

The Examiner submits in Office Action B, 3:24 - 3:27, that the prior art motivation or advantage may be different than that of Applicant's while still supporting a conclusion of obviousness. (*In Re Wiseman*, 201 USPQ 658 (CCPA); *Ex Parte Obiaya* 227 USPQ 58 (Board of App. 1985). However,

while the Applicant agrees with the Examiner that the motivation of McTeer in reducing voids is different than the Applicant's motivation in passivating structural defects in a silicon layer, there is nothing in McTeer that makes up for the fact that McTeer does not anywhere teach or suggest that the final anneal operates "so that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit". It is a well-established principle that the mere absence from a reference of an explicit requirement of the claim cannot reasonably construed as an affirmative statement that the requirement is in the reference. *In re Evanega*, 829 F.2d 1110, 4 USPQ2d 1249 (Fed. Cir. 1987). In summary, because a teaching or suggestion of either "further heating the integrated circuit ... *so that impurities from the dielectric layer have passivated structural defects* within a silicon layer of the integrated circuit" or "further heating the integrated circuit at 400 degrees C for about 45 minutes" is completely absent from McTeer, McTeer cannot be used to meet the Applicant's recited limitation of "further heating the integrated circuit at 400 degrees C for about 45 minutes so that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit". Again, the prima facie case has not been met.

As asserted by the Examiner in Office Action B, 2:22 - 3:3, such heating at 400° C for about 45 minutes would come about as a result of experimentation and optimization of the McTeer process. However, since the McTeer process is directed at reducing the structural voids and not at utilizing the impurities from the dielectric layer to passivate structural defects within a silicon layer, it cannot be said that experimentation and optimization of the McTeer process would result in the temperature and duration requirements recited in Applicant's claim 1 of "further heating the integrated circuit at 400 degrees C for about 45 minutes". The Examiner has not pointed to anything in McTeer or any other prior art that indicates that experimenting with heating temperatures and durations to cure the defects within the layers (McTeer, 4:34 - 4:38) would lead to trying 400° C for about 45 minutes. Thus, even through experimentation, it cannot be said that the Applicant's claimed step of "further heating the integrated circuit at 400 degrees C for about 45 minutes" would be rendered obvious in view of McTeer.

The Examiner submits in Office Action B, 4:2- 4:4 that the Applicants

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have not proved that the heating temperature and heating duration are critical or produce an unexpected result. However, as described above, the Examiner has not met the prima facie case of obviousness as to Applicant's claim 1. Accordingly, the burden of proof has not yet shifted to the Applicant for providing such proof.

The Examiner further submits in Office Action B, 4:4 - 4:5 that the claimed temperature and duration would produce the expected result of curing defects as taught by McTeer. However, McTeer does not specify what the temperature and duration are that would result in curing the defects in the layers. Therefore, the Applicant does not understand from where the Examiner receives such knowledge and respectfully requests the Examiner to please specify so that the Applicant can form a proper response.

For the above reasons, the Applicants believe that claim 1 is not made unpatentable by McTeer, and is thus allowable. Also, since claims 2, 3, and 4 depend from claim 1, they incorporate the limitations from independent claim 1 that are missing from McTeer and the prior art. Therefore, the Applicants believe that claims 2, 3, and 4 are allowable as well.

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Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 1-4 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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January 19, 2005

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